PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/21/13053
1.3 Title of PCN	STL120N8F7 (OD8F): Metal and Passivation Change
1.4 Product Category	STL120N8F7
1.5 Issue date	2021-10-10

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	NEMETH KRISZTINA
2.1.2 Phone	+49 89460062210
2.1.3 Email	krisztina.nemeth@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Mario ASTUTI
2.1.2 Marketing Manager	Anna RANIOLO,Michele SCUTO
2.1.3 Quality Manager	Vincenzo MILITANO

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Wafer Fab (Process)	Metallization : change in metal layers type/nature, composition or final thickness	ST AngMoKio (Singapore)

4. Description of change		
	Old	New
4.1 Description	Metal: TiAlCu 4.5 um Passivation: TEOS 10 kA + Sin 10kA	Metal: TiAlCu 3.2 um Passivation: USG 6 kA + TEOS 12 kA
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	Fab Process Rationalization
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	Dedicated Finished Good Code

7. Timing / schedule	
7.1 Date of qualification results	2021-10-01
7.2 Intended start of delivery	2022-01-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13053 Validation.zip		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-10-10

9. Attachments (additional documentations)
13053 Public product.pdf 13053 Validation.zip 13053 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STL120N8F7	

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PRODUCT/PROCESS CHANGE NOTIFICATION

TITLE	**STL120N8F7 (OD8F): Metal and Passivation Change**
IMPACTED PRODUCTS	STL120N8F7 (silicon line OD8F)
MANUFACTURING STEP	Silicon Diffusion (Metal and passivation steps)
INVOLVED PLANT	ST SG8" (AngMoKio – Singapore)
CHANGE REASON	Fab Process Rationalization
CHANGE DESCRIPTION	Due to process rationalization on STL120N8F7 (silicon line OD8F) Will be introduced the following metal and passivation changes

	Current	New
Metal	TiAlCu 4.5 um	TiAlCu 3.2 um
Passivation	TEOS 10 kA + Sin 10kA	USG 6 kA + TEOS 12 kA

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TRACEABILITY	Dedicated Finished Good codes
VALIDATION	Qualification results (reliability, electrical comparison) included in this communication
REPORTS	13053_Validation.zip

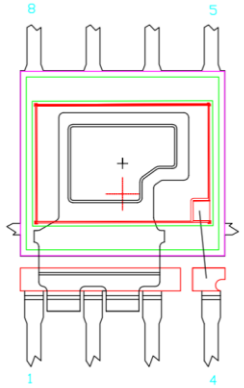
STL120N8F7 (OD8F01): Fab Process Rationalization

Release date: October, 2021

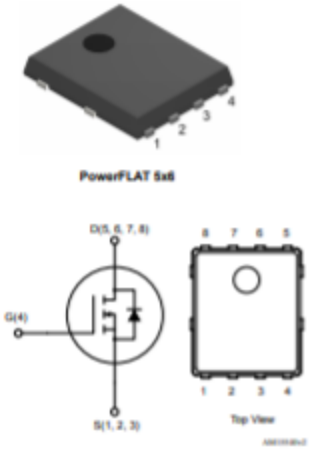
OUTLINE

Description of the change

Commercial Product	Silicon Line	PACKAGE	Techno	Change Description
STL120N8F7	OD8F01	Power FLAT 5x6	OFT1 80V	• Industrial vs Automotive FE process integration and rationalization – Metal and Passivation alignment



OD8F (10 mm²)



STL120N8F7
Change Details Table

Item	Changed	Current	Proposal
Wafer Production Site	**YES**	AMK – SG8 FAB	AMK – SG8 FAB
Materials	NO		
Production Method	NO		
Layout	NO		
Mask (active area)	NO		
Metal layer	**YES**	TiAlCu 4.5 um	TiAlCu 3.2 um
Passivation layer	**YES**	TEOS 10 kA + Sin 10kA	USG 6 kA + TEOS 12 kA
Passivation mask	NO		
Brasable Metal	NO		
Wafer Probe Test	NO	ST AMK (Singapore) EWS	ST AMK (Singapore) EWS
Package Assembly Site	NO	Same Assembly Plant → NANTONG FUJITSU (TFME) - CHINA	
Wafer Mount & Sawing	NO		
Die Attach	NO		
Wire Bonding	NO		
Molding	NO		
Cropping	NO		
Final Testing	NO	Same Testing Plant → NANTONG FUJITSU (TFME) - CHINA	

Qualification Plan for AMK Silicon

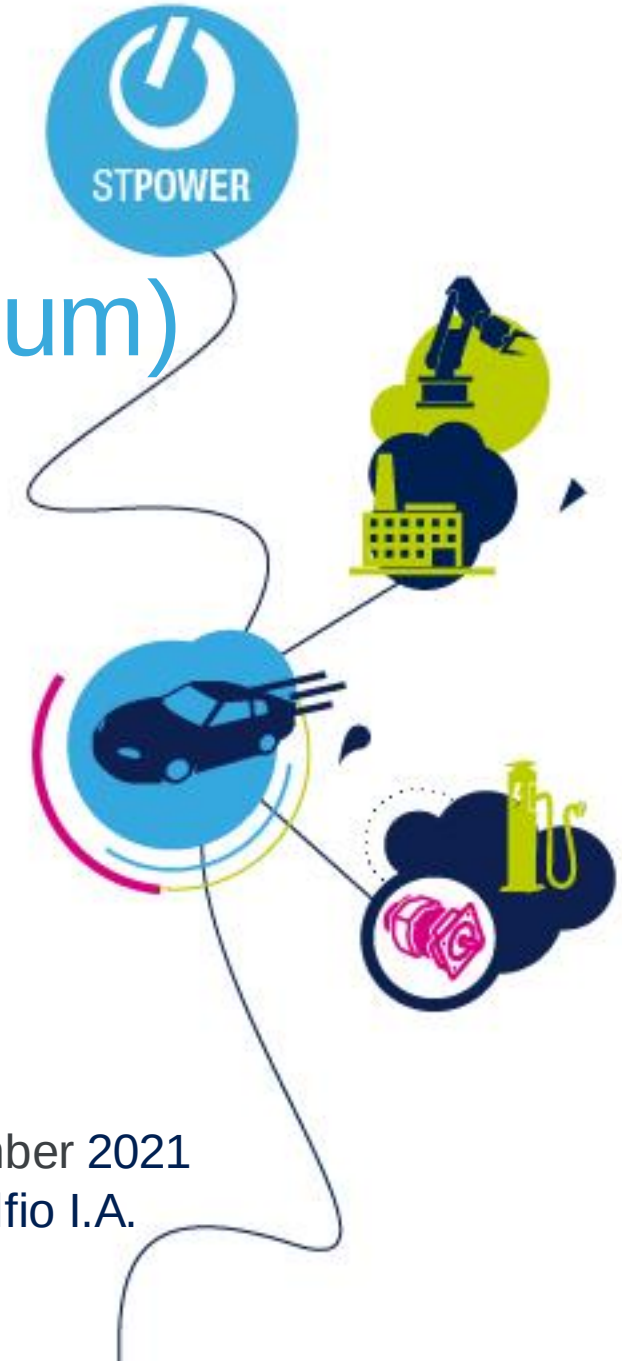
Silicon Line	Die size	Commercial Product	Package	Sample Size	Target	Qualification Plan
OD8F	10.4mm²	STL120N8F7	PowerFlat 5x6	1 Lot	Full Product Qualification	• Static and Reliability electrical parameters - Comparative analysis with Catania

AEC-Q101 Test Plan Table

#	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
1	TEST	Pre- and Post- Stress Electrical Test	Yes
2	PC	Preconditioning	Yes
3	PV	Parametric Verification	Yes
4	HTRB	High Temperature Reverse Bias	Yes
5	HTGB	High Temperature Gate Bias	Yes
	HTGB(n)	High Temperature Gate Bias – negative	Yes
6	HTSL	High Temperature Storage Life	Yes
7	THB	Temperature Humidity bias	Yes
8	AC	Autoclave	Yes
9	TC	Temperature Cycling	Yes
10	IOL	Intermittent Operational Life	Yes
11	ESD -HBM	Human Body Model ESD	Yes
12	ESD – CDM	Charged Device Model ESD	Yes

Thank you

OD8F080 (3.2 um) vs OD8FRH8 (4.5 um)
Product : STL120N8F7
Package : PowerFLAT 5x6



ADG SUPPLY CHAIN & OPERATIONS

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29 September 2021

Messina Alfio I.A.

FINAL TESTING

					3.2u					4.5u							
Test label	Unit	LTL		UTL	Mean	Sigma	CPK L	CPK H	CPK	Mean	sigma	CPK L	CPK H	CPK	delta[meanRP-meanSP]	2sigmaSP	Check
BVdss 1mA	V	80.0		90.0	92.2000	0.4000	10.17	1.83	1.83	91.4900	0.2800	13.68	1.77	1.77	0.710	0.800	TRUE
Vth_250uA	V	2.50		4.50	3.7900	0.1410	3.05	1.68	1.68	3.5400	0.1490	2.33	2.15	2.15	0.250	0.282	TRUE
Idss 60V	nA	-1000.0		1000.0	3.7000	2.4000	139.40	138.38	138.38	4.5400	6.6300	50.50	50.05	50.05	0.840	4.800	TRUE
Igss 20V	nA	-100.0		100.0	11.8000	6.1300	6.08	4.80	4.80	11.9000	6.4000	5.83	4.59	4.59	0.100	12.260	TRUE
Igss -20V	nA	-200.0		200.0	12.7100	8.7300	8.12	7.15	7.15	14.2000	11.4000	6.26	5.43	5.43	1.490	17.460	TRUE
Vdson 20A	mV	0.0		55.2	45.3900	1.4800	10.22	2.21	2.21	42.4900	1.1400	12.42	3.72	3.72	2.900	2.960	TRUE
Vsd 40A	V	-1.2		0.0	0.7530	0.0163	39.94	15.40	15.40	0.7730	0.0326	20.17	7.90	7.90	0.020	0.033	TRUE

EWS

					3.2um					4.5um							
Test label	Unit	LTL		UTL	Mean	Sigma	CPK L	CPK H	CPK	Mean	sigma	CPK L	CPK H	CPK	delta[meanRP-meanSP]	2sigmaSP	Check
BVdss 1mA	V	80.0		120.0	92.5100	1.3000	3.21	7.05	3.21	92.5800	1.6100	2.60	5.68	2.60	0.070	2.600	TRUE
Vth_250uA	V	2.50		4.50	3.6400	0.1350	2.81	2.12	2.12	3.7900	0.1340	3.21	1.77	1.77	0.150	0.270	TRUE
Idss 81V	nA	-800		800	3.3000	2.4000	111.57	110.65	110.65	4.5000	3.9000	68.76	67.99	67.99	1.200	4.800	TRUE
Igss 21V	nA	-100.0		100.0	2.5000	1.9000	17.98	17.11	17.11	3.3000	2.8000	12.30	11.51	11.51	0.800	3.800	TRUE
Igss -21V	nA	-200.0		200.0	2.6000	1.8000	37.52	36.56	36.56	3.4000	2.9000	23.38	22.60	22.60	0.800	3.600	TRUE
Vdson 10A	mV	-500.0		500.0	38.1900	4.9900	35.95	30.85	30.85	41.9100	5.9400	30.41	25.71	25.71	3.720	9.980	TRUE
Vsd 10A	V	0.0		1.2	0.7900	0.0045	58.52	30.37	30.37	0.7950	0.0055	48.18	24.55	24.55	0.005	0.009	TRUE

Reliability Evaluation Report
STL120N8F7 (OD8F01)
New Product Qualification

General Information	
Commercial Product	**STL120N8F7**
Product Line	**OD8F01**
Silicon process Technology	**F7 OFT1 80V**
Package	**PowerFLAT 5x6**

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive and Standard Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

Rev.	Change description	Author	Date
1.0	New release	A. Giuffrida	10h June 2021

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	A. Marmoni	10h June 2021

Table of Contents

1. Reliability Evaluation Overview

1.1. Objective

Aim of this report is to present the results of the reliability evaluations performed on **STL120N8F7** (OD8F01 as ST internal silicon line) to release the products to commercial maturity. These are N-channel PowerMOSFET designed in F7 OFT1 80V Power MOSFET Technology, diffused in ST SG8 Ang Mo Kio (Singapore) 8" Wafer Fab, assembled in PowerFLAT5x6 in Tongfu Microelectronics TFME (China) subcon assembly plant.

Reliability Strategy and Test Plan

1.2. Reliability strategy

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.2.1. Test Plan

Test Plan Table

#	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
1	TEST	Pre- and Post- Stress Electrical Test	Yes
2	PC	Preconditioning	Yes
3	PV	Parametric Verification	Yes
4	HTRB	High Temperature Reverse Bias	Yes
5	HTGB	High Temperature Gate Bias	Yes
	HTGB(n)	High Temperature Gate Bias - negative	Yes
6	HTSL	High Temperature Storage Life	Yes
7	THB	Temperature Humidity bias	Yes
8	AC	Autoclave	Yes
9	TC	Temperature Cycling	Yes
10	IOL	Intermittent Operational Life	Yes
11	ESD -HBM	Human Body Model ESD	Yes
12	ESD - CDM	Charged Device Model ESD	Yes

1.3. Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

Based on the overall positive results obtained the product **STL120N8F7** (OD8F01 as ST internal silicon line) diffused in ST SG8 Ang Mo Kio (Singapore) 8" Wafer Fab, assembled in PowerFLAT5x6 in Tongfu Microelectronics TFME (China) subcon assembly plant, has positively passed reliability evaluation performed in agreement with **ST 0061692** specification.

2. Product Characteristics

2.1. Generalities

2.1.1. Test vehicle

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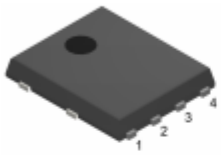
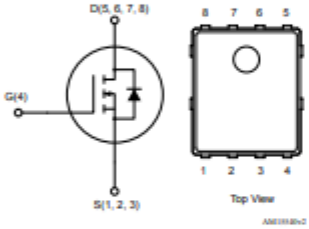
STL120N8F7

Datasheet

N-channel 80 V, 4.0 mΩ typ., 120 A STripFET F7 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL120N8F7	80 V	4.8 mΩ	120 A	140 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

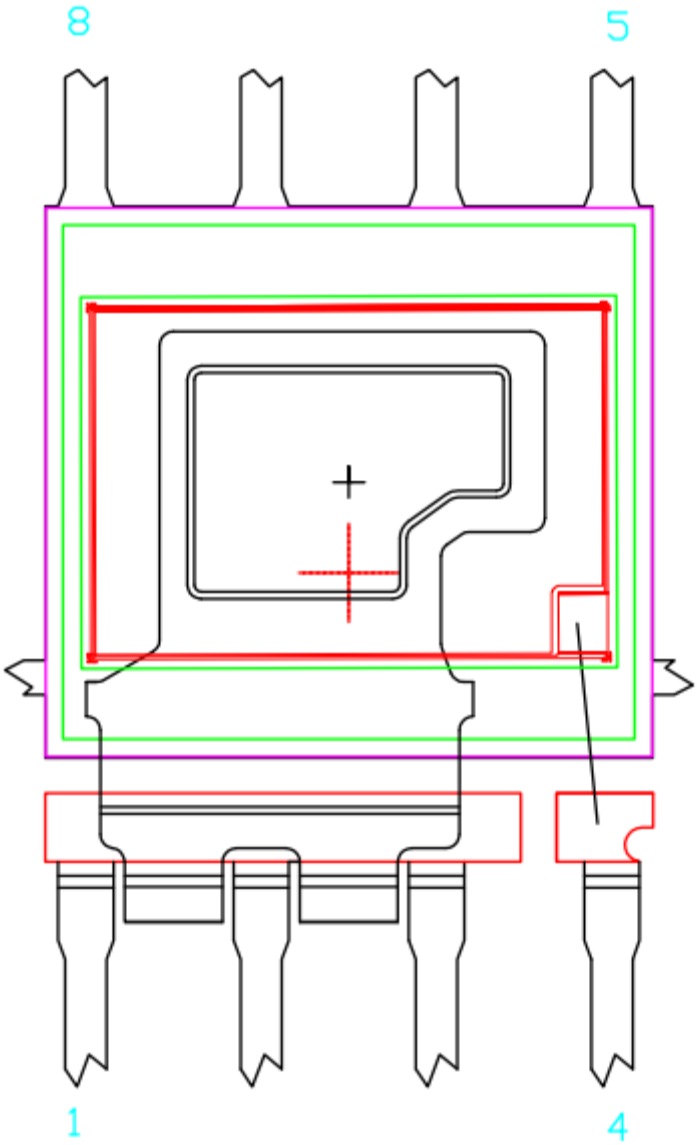
This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

STPOWER

Product status link
STL120N8F7

Product summary	
Order code	STL120N8F7
Marking	120N8F7
Package	PowerFLAT 5x6
Packing	Tape and reel

2.2. Pin Connection/Bonding Diagram



2.3. Traceability

2.3.1. Wafer Fab information

Wafer fab name / location	ST Ang Mo Kio SG8 (Singapore)
Wafer diameter (inches)	8”
Silicon process technology	OFT1 80V
Die finishing front side	USG + TEOS
Die finishing back side	Ti-NiV-Ag
Die size (micron)	2700 x 3880 um
Metal levels/ materials/ thicknesses	TiAlCu (3.2um last level)

2.3.2. Assembly Information

Assembly plant name / location	NANTONG FUJITSU (TFME) - CHINA
Package description	PowerFLAT 5x6
Lead frame/Substrate	PDFN8R 157*173 ASM
Die attach material	PbSn5Ag2.5-D3-RM218-8
Wire bonding material/diameter	PDFN BIG CLIP (AA) LOW THK Wires 2 mils Au
Molding compound material	CEL9220HF10 HITACHI
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1

2.3.3. Reliability Testing Information

Reliability laboratory location	STM Catania (Italy)

3. Test summary details

3.1. Lot Information

Lot #	Diffusion Lot	Assembly Lot	Note
Lot1	C9399XL	GF013479	BSUO*OD8F08F

3.2. Test Summary table

Test method revision reference is the one active at the date of reliability trial execution.

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
TEST	1		User specification or supplier's standard specification	1	539	539	0/539/1	All qualification parts
PC	2	JEDEC/IPC J-STD-020 JESD22-A-113	MSL1: 168h moisture soak @ 85°C RH=85% 3x Reflow simulation with Peak Reflow Temp= 260°C	-	308	308	0/308/1	All parts before TC, AC, THB, IOL
PV	4	-	All parameters	1	25	25	Done	
HTRB	5	MIL-STD-750-1 M1038 Method A	1000h @ Tj=175°C, Vds=80V	1	77	77	0/77/1	
HTGB	6	JESD22 A-108	HTGB 1000h @ Ta=175°C Vgs= 20V	1	77	77	0/77/1	
HTSL	7	JESD22A103	1000h @ Ta=150°C	1	45	45	0/45/1	
THB	8	JESD22A-101	1000h @ Ta=85°C, RH=85% Vds =64V	1	77	77	0/77/1	
AC	9	JESD22 A-102	AC (Ta=121°C, Pa=2atm for 96 hours)	1	77	77	0/77/1	
TC	10	JESD22A-104 Appendix 6 J-STD-035	Ta=-55°C /+150°C Duration= 1000cy	1	77	77	0/77/1	
IOL	11	MIL-STD-750 Method 1037	10Kcy @ Ta=25°C with parts powered to insure $\Delta Tj \geq 100°C$	1	77	77	0/77/1	
ESD - CDM	12	CDM	Charge Device Model	1	3	3	Done	
ESD -HBM	13	HDM	Human Body Model	1	3	3	Done	

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